Figure 1. 3D-quarter model of JEDEC board (Solder bump model)

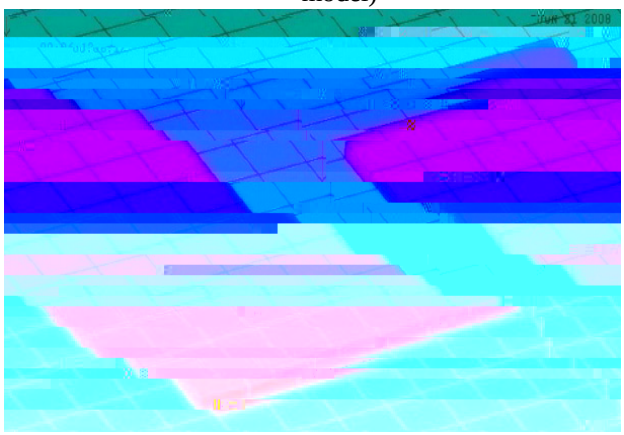


Figure 2 Details at Solder Layer model

**4.1(b) Transient Dynamic Analysis**

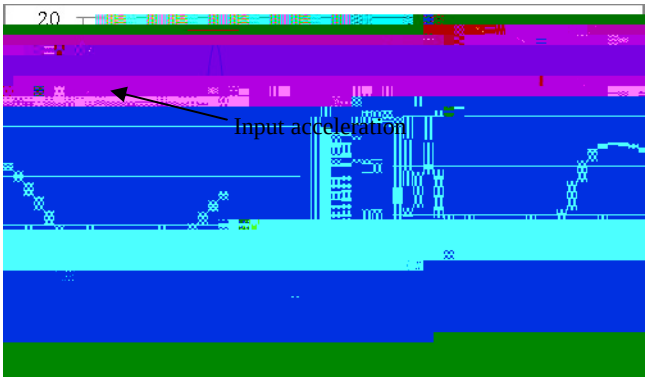



Figure 5. Comparison for input G and input acceleration methods

The board strain along path 1-3 at t=1.5 ms are plotted in Figures 6 and 7. As is seen that the same results are obtained for input G and input acceleration method.

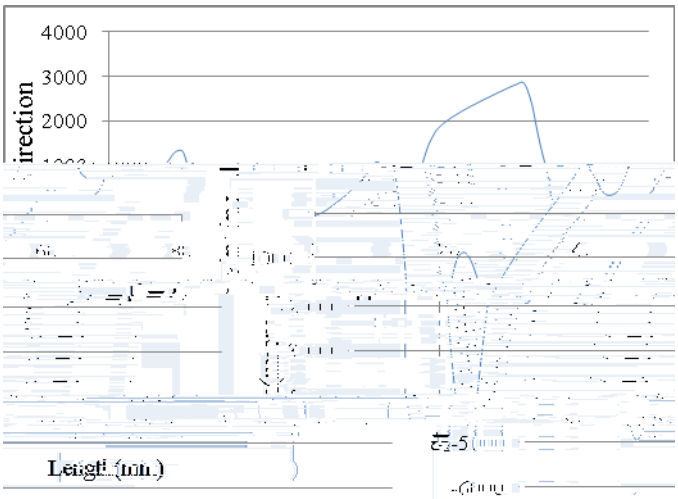



Figure 6. Board strain for input G method (full dynamics)

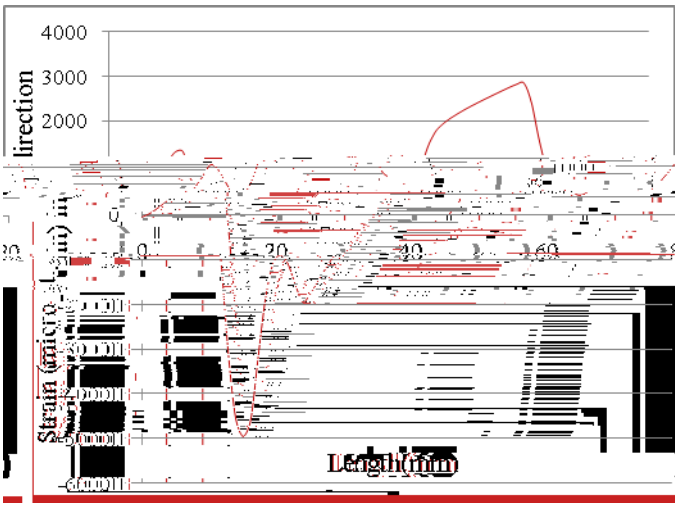



Figure 7. Board strain for input acceleration method (full dynamics)

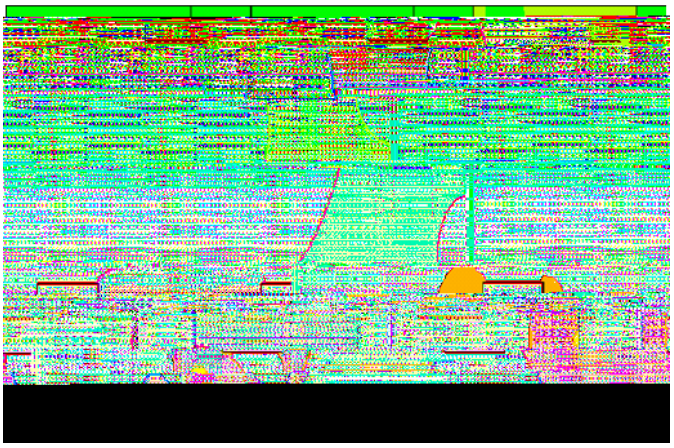
### 4.3 Comparison of Full Dynamics and Mode-Superposition Method

The board strains calculated with both full dynamics and mode-superposition methods are is plotted in Figure 8. It is seen that board strains obtained with both solution methods have the same trend. However, peak value of strain is different. It is approximately 5000 micro-strain for full dynamics while it is approximately 4000 micro-strain for mode-superposition method. The board strain and displacement (in z-direction) obtained with the two methods are plotted in figures 9 and 10. It can be seen that solutions with both methods follow the same trends. However, the magnitudes of strain and displacement solutions with these two methods are different. The mode-superposition method always seems to give numerically less value than the full transient analysis.

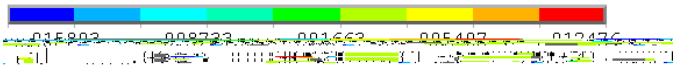
It is observed from Figures 9 and 10 that the maximum elastic strain occurs near the mounting hole, while the board center has the most deflection. Furthermore, the mounting hole region is bent in the opposite direction compared to the board center.

It should be pointed out here that there are some problems regarding post-processing in ANSYS for the mode-superposition method. The acceleration-time history cannot be plotted. It is sometimes difficult to obtain strain history plots as well. In addition, it takes longer time to post process obtain the full solution by expansion (using EXPASS command). The mode-superposition occupies more memory space than full dynamics. For a case studied, with 6x6mm chip size, mode-superposition method takes more than 4 times the memory space than that of full dynamics. The full dynamics, on the other hand, takes longer time to calculate the full solution. However, it takes overall shorter time since the post processing is fast. Therefore, full dynamics approach is preferred.

Figure 8. Comparison of board strain full dynamics and mode-superposition method



Board strain in x-direction at time 1.5 ms
Full dynamics analysis method



Mode superposition
method

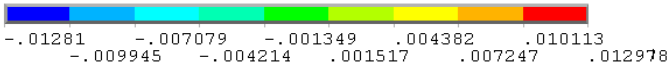
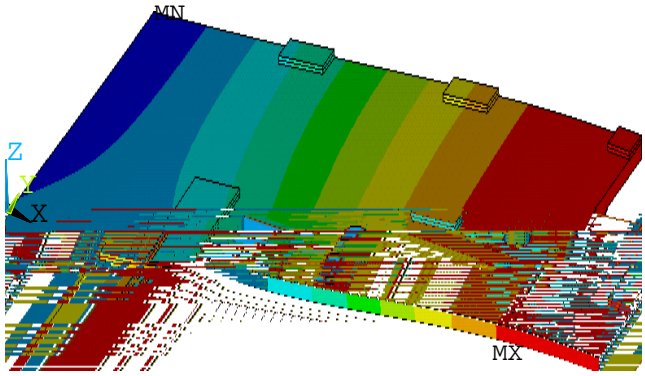
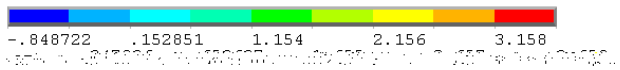



Figure 9. Comparison of board strain for input acceleration and input G

Fig. 11 and 12 plot elastic strain history at location 1 and location 6, respectively for both strains in x- and y- direction. We can see that strain components in x-direction and y-direction at the board corner (1mmx1mm from U1) are much higher than those at board center (1mmx1mm from U8) and bending direction is opposite. Strain in y-direction has higher frequency than the strain in x-direction.




Board displacement in z-direction at time 1.5 ms
Full dynamics analysis method




Mold-superposition Method

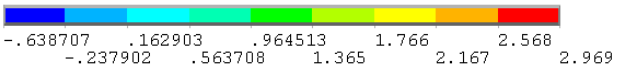



Figure10. Comparison of board displacement (in z-direction) for full dynamics and mode-superposition method

The board displacements in x and y directions for site 1 and 6 (figure 1) are plotted in figures 11 and 12. There are two three observations:

a. the strain in x direction is dominant
b. the strain components in both x and y directions are opposite between locations 1 and 6.
c. Strain component is x direction correspo ie st and mao8( lo)5(eal ( lo)5(m)9.7(iu lo)5(ral 3(qqu lo)5(rp)-2(( lo)5(c

reduces the computational type by 2/3, compared to 20- node element. Such results are observed differently when ABAQUS software is used [15].

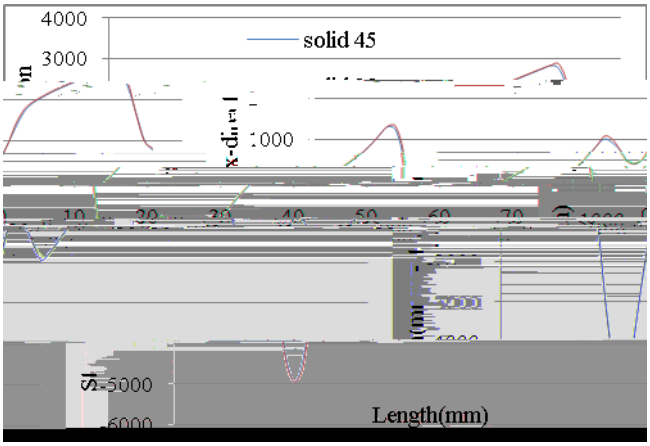



Figure13. Comparison of board strain for 8 node and 20 node elements

## 5. Results and Discussions

### 5.1 Effect of the Boundary Condition at Mounting Hole on System Natural Frequency

The boundary conditions at mounting the hole have some effect on the natural frequencies of the system. A 6x6 mm chip size model is studied for this effect. Two types of boundary conditions are considered. The first one is fixing displacement in z-direction only. The second boundary condition is fixing displacement in all directions at mounting hole. The natural frequencies obtained from models with these two different boundary conditions are listed in table 3. It is seen that slightly higher natural frequencies are obtained when displacements of all directions are fixed at mounting hole. This is due to the fact that the board becomes less flexible under this boundary condition. Overall, the fundamental frequency is from 200 to 250 Hz, which is consistent with many test results.

Table 3. Effect of boundary conditions on natural frequency of the model

| Mode No. | Natural frequency (Hz) | |
|---|---|---|
| | Only Z direction is fixed | All (X,Y,Z) are fixed |

not significant. The detailed study on the effect of chip size on solder joint stress will be reported in the future.

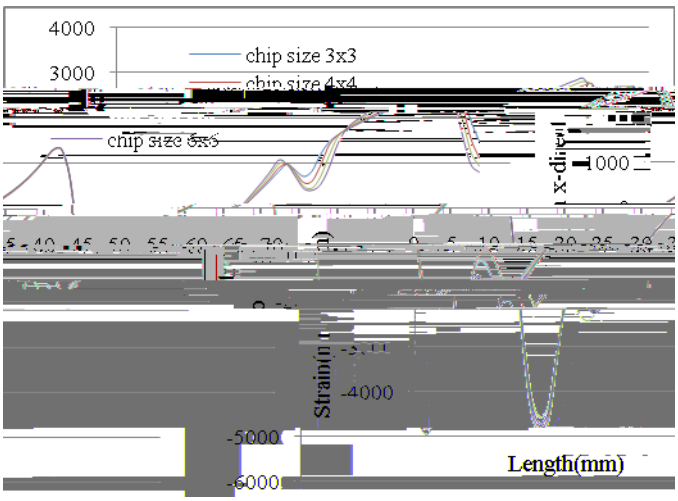



Figure18. Comparison of board strain for different chip sizes

### 5.6 Effect of Boundary Conditions for Direct Input Acceleration Method

In order to assess the effect of boundary conditions, two boundary conditions at mounting hole are considered. This first case incorporates displacemet components in x, y, and z directions for nodes at the mounting hole being fixed. The second case incorporates displacement in z-direction only is fixed for nodes at the mounting hole. The models with these two sets of bondary conditions are studied with input acceleration method. The board strain is plotted in figure 19. It is seen that slightly different results are obtained for the two different boundary conditions. The theoretical study on the model study will be reported in the future.

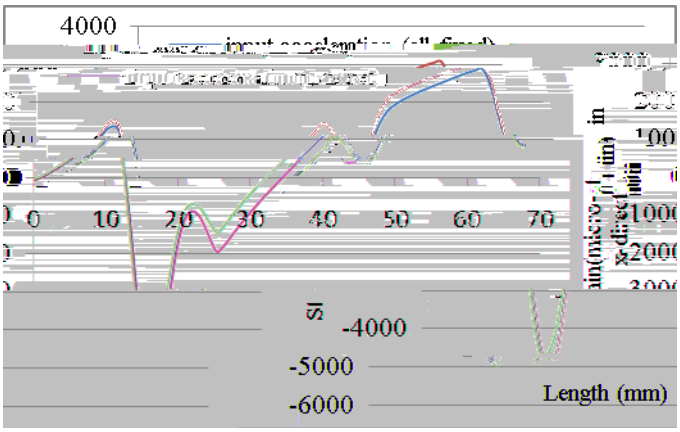



Figure 19. Comparison of board strain for different boundary conditions in input acceleration method.

### 6. Conclusions

Based on the studies in this paper, it is recommended that, in order to achieve the computational efficieny without the loss of accuracy, a solder layer model for wafer-level packages with direct acceleration input using full transient implicit anaysis provides an accurrate and fast board dynamic response analysis. The mode superposition in ANSYS does not have an advantage in saving computation time since the

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13. Loh Wei Keat; Lee Yung Hsiang; Ajay Munigayah; Tay Tiong We, “Nonlinear dynamic behavior of thin PCB board for solder joint reliability study under shock loading”, International Symposium on Electronics Materials and Packaging, 11-14 Dec. 2005 Page(s): 268 - 274
14. Lianxi Shen, “Simulation of drop test board with 15 components using explicit and implicit solvers”, 2008 International ANSYS Conference August 26 to 28 in Pittsburgh, Pennsylvania, U.S.A.
15 Xuejun Fan; Min Pei, and Pardeep K. Bhatti, “Effect of finite element modeling techniques on solder joint fatigue life prediction of flip-chi